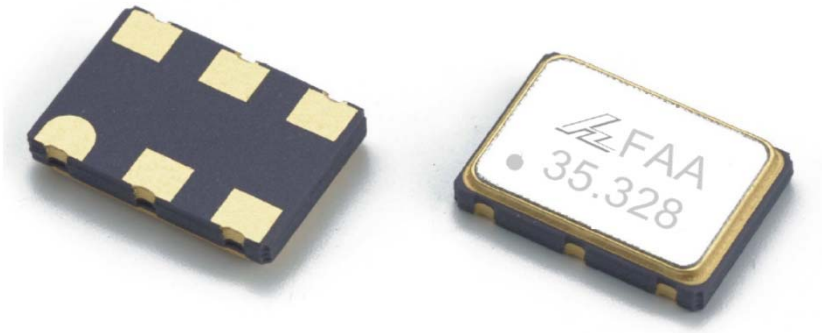
PECL Oscillator (7.0x5.0) SMD Type

Application of Oscillator

- PLL circuit
- Broad casting equipment
- AFC circuit
- Sonet/SDH.ATM
- FM modulator



Features

- Wave form symmetry of 40/60%
- PECL output
- Industry standard 6 Pad 5 x 7 Ceramic SMD Package
- Supply voltage of 3.3 and 5.0 VDC deliverable
- Low Jitter 1.0 ps max
- Rohs compliant / Pb free

RoHS

Electrical Specification

PARAMETERS	CONDITIONS	CHARACTERISTICS		UNITS
Output Logic	-	Positive ECL Square Wave (PECL)		-
Input Voltage (VDD)	-	3.3 ±10%	5.0 ±10%	VDC
Frequency Range (fO)	-	19.440 ~ 180.0 (Fund, Third, Fifth /		MHz
Operating Temperature (TOPR)	-	0 ~ +70 (Std.) / -40 ~ 85 (Option)		°C
Storage Temperature (TSTG)	-	-55 ~ +125		°C
Overall Frequency Stability	-	±50, ±100 max.		PPM
	(a) Frequency Tolerance	Inclusive of Overall Stability		-
	(b) Temperature Stability	Inclusive of Overall Stability (Operating Temperature)		-
	(c) Input Voltage Stability	Inclusive of Overall Stability (VDD ± 10%)		-
	(d) Load Stability	Inclusive of Overall Stability (RL ±		-
Input Current (IDD)	-	80 max.	120 max.	mA
Aging	@ 25°C	±3 max.		PPM/Y
Rise Time (TR)	20% to 80% of Waveform	2 max.		nS
Fall Time (TF)	20% to 80% of Waveform	2 max.		nS
Output Voltage High "1" VOH	PECL	VDD - 1.025 min.		VDC
Output Voltage Low "0" VOL	PECL	VDD - 1.620 max.		VDC
Load	-	50		Ohms
Duty Cycle	50% of Waveform	50 ±10 (Std.) / 50 ±5 (Option)		%
Start-Up Time (TS)	-	10 max.		mS
Jitter	Fj 12KHz to 20MHz bandwidth	1.0 max.		ps

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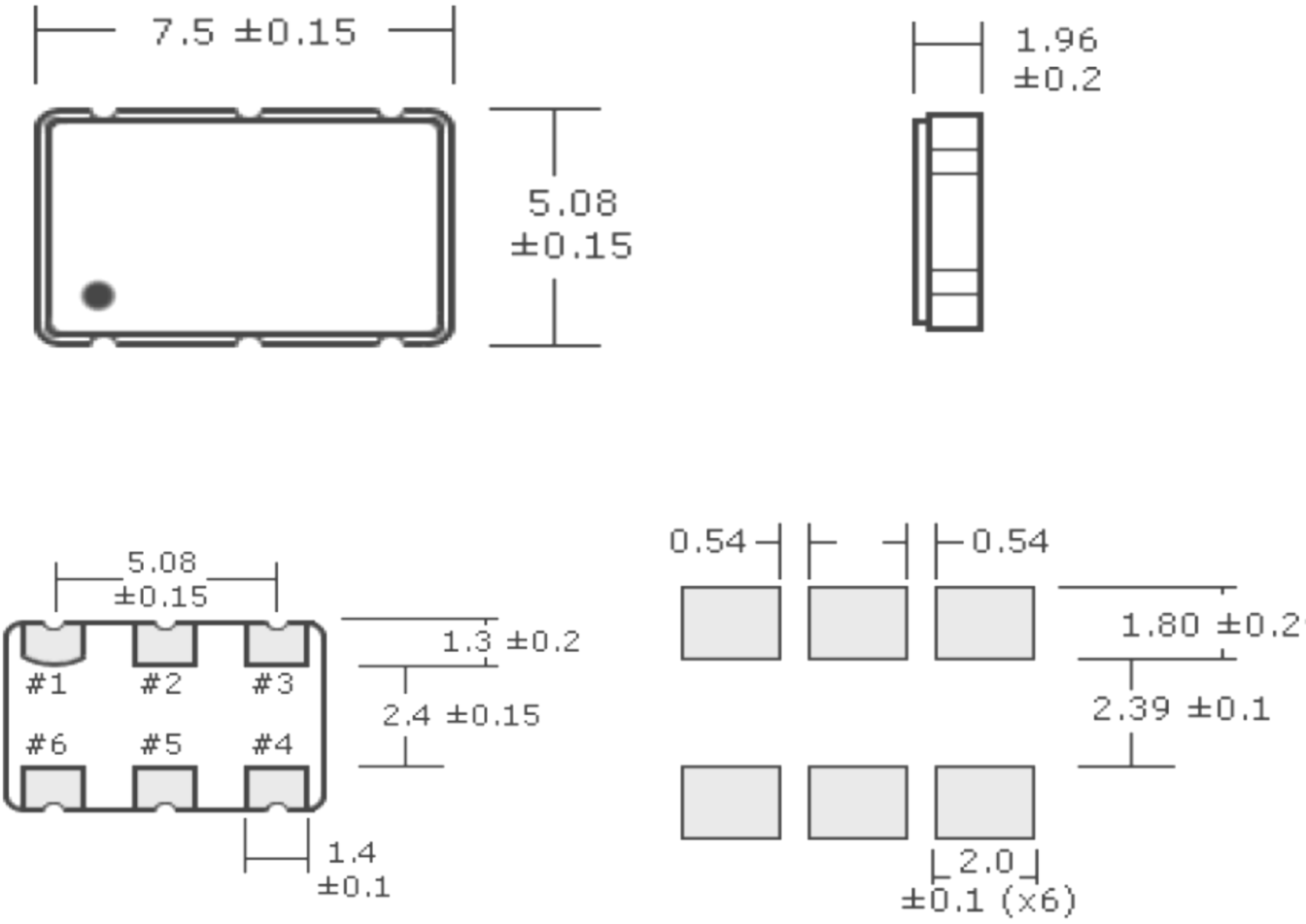
Dimensions (mm):



PIN CONNECTIONS	
#1	Tristate Enable High or No Connection (TS1)
#2	Tristate Enable High or No Connection (TS)
#3	Ground
#4	Output
#5	Complimentary Output
#6	Vdd